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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/773,543	02/02/2001	Shunpei Yamazaki	12732-012001 / US4638	8040

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EXAMINER
MANDALA, VICTOR A

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 08/14/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

CH

Office Action Summary	Application No.	Applicant(s)	
	09/773,543	YAMAZAKI ET AL.	
	Examin r	Art Unit	
	Victor A Mandala Jr.	2826	

-- The MAILING DATE of this communication appears on th cover sheet with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 May 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *28-37* is/are allowed.

6)☒ Claim(s) *1,3,5,6,8-10,12,15,16,18-21,24,25 and 27* is/are rejected.

7)☒ Claim(s) *2,4,7,11,13,14,17,22,23 and 26* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1, 3, 5-6, 8-9, 10, 12, 15-16, 18-21, 24-25, & 27 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,469,317 Yamazaki et al.

The applied reference has common inventors with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

1. Referring to claim 1, a semiconductor device comprising: a semiconductor layer, (Figure 17 #1704-1712), formed on an insulating surface, (Figure 17 #1702), and having at least a source region, (Figure 17 #1704), a drain region, (Figure 17 #1712), and a channel formation region, (Figure 17 #1706 & 1710), interposed there-between; a first insulating film, (Figure 17 examiner's label #6), formed on said semiconductor layer, (Figure 17 #1704-1712); at least one electrode, (Figure 17 #1718), formed on said first insulating film, (Figure 17 examiner's label #6), and overlapping said channel formation region, (Figure 17 #1706 & 1710); a source wiring,

(Figure 17 #1723), formed on said first insulating film, (Figure 17 examiner's label #6); a second insulating film, (Figure 17 #1727), covering at least said at least one electrode, (Figure 17 #1718), and said source wiring, (Figure 17 #1723), and a gate wiring, (Figure 17 #1716), formed on said second insulating film, (Figure 17 #1727), and connected to said at least one electrode, (Figure 17 #1718).

2. Referring to claim 3, a semiconductor device, wherein said at least one electrode, (Figure 17 #1718), comprises a gate electrode, (Figure 17 #1718).

3. Referring to claim 5, a semiconductor device, wherein a material of said gate wiring, (Figure 17 #1716), comprises one or a plurality of elements selected from the group consisting of polySi, W, WSi, At, Cu, Ta, Cr and Mo, (Col. 17 Lines 45-47 & Figures 9A & 11).

4. Referring to claim 6, a semiconductor device, wherein said first insulating film, (Figure 17 examiner's label #6), comprises a gate insulating film, (Figure 17 examiner's label #6).

5. Referring to claim 8, a semiconductor device, wherein said group consisting of a personal computer, a semiconductor device is one selected from the video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 33).

6. Referring to claim 9, a semiconductor device comprising: a semiconductor layer, (Figure 17 #1704-1712), formed on an insulating surface, (Figure 17 #1702), and having at least a source region, (Figure 17 #1712), a drain region, (Figure 17 #1705), and a channel formation region, (Figure 17 #1706 & 1710), inter-posed there-between; a first insulating, (Figure 17 examiner's label #6), formed on said semiconductor layer, (Figure 17 #1705-1711); at least one electrode, (Figure 17 #1718), formed on said first insulating film, (Figure 17 examiner's label #6), and

overlapping said channel formation region, (Figure 17 #1706 & 1710); a source wiring, (Figure 17 #1724), formed on said first insulating film, (Figure 17 examiner's label #6); a second insulating film, (Figure 17 #1727), covering at least said at least one electrode, (Figure 17 #1718), and said source wiring, (Figure 17 #1724), a gate wiring, (Figure 17 #1718), formed on said second insulating film, (Figure 17 #1727), and connected to said at least one electrode, (Figure 17 #1718); a connection electrode, (Figure 17 examiner's label #7), formed on said second insulating film, (Figure 17 #1727), and connected to said source wiring, (Figure 17 #1724),and said semiconductor layer, (Figure 17 #1704-1712); and a pixel electrode, (Figure 17 #1728), formed on said second insulating film, (Figure 17 #1727), and electrically connected to said semiconductor layer, (Figure 17 #1704-1712).

7. Referring to claim 10, a semiconductor device, wherein said pixel electrode, (Figure 17 #1728), overlaps said source wiring, (Figure 17 & 1724).

8. Referring to claim 12, a semiconductor device, wherein said at least one electrode comprises a gate electrode, (Figure 17 #1718).

9. Referring to claim 15, a semiconductor device, wherein a material of said gate wiring comprises one or a plurality of elements selected from the group consisting of polySi, W, WSix, Al, Cu, Ta, Cr and Mo, (Col. 17 Lines 45-47 & Figures 9A & 11).

10. Referring to claim 16, a semiconductor device, wherein said first insulating film comprises a gate insulating film, (Figure 17 examiner's label #6).

11. Referring to claim 18, a semiconductor device, wherein one pixel including said pixel electrode, (Figure 17 A&B #1728), forms a storage capacitor between said semiconductor layer, (Figure 17 A&B #1704-1712), connected to said pixel electrode, (Figure 17 A&B #1728), and

said at least one electrode, (Figure 17 A&B #1718), connected to a gate wiring, (Figure 17 A&B #1716), of an adjacent pixel, using said first insulating film, (Figure 17 examiner's label #6), as a dielectric.

12. Referring to claim 19, a semiconductor device, wherein an impurity element for imparting a p-type conductivity, (Col. 26 Lines 10-11), is added to said semiconductor layer, (Figure 17 #1705-1711), connected to said pixel electrode, (Figure 17 # 1728).

13. Referring to claim 20, a semiconductor device, said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 33).

14. Referring to claim 21, a semiconductor device comprising: a first insulating film, (Figure 17 examiner's label #6), adjacent to a semiconductor layer, (Figure 17 #1704-1712), said semiconductor layer, (Figure 17 #1704-1712), having at least a source region, (Figure 17 #1712), a drain region, (Figure 17 #1704), and a channel formation region, (Figure 17 #1706 & 1710), interposed there-between; at least one electrode, (Figure 17 #1723), including a gate electrode, (Figure 17 #1718), formed on said first insulating film, (Figure 17 examiner's label #6); a source wiring, (Figure 17 #1724), formed on said first insulating film, (Figure 17 examiner's label #6); a second insulating film, (Figure 17 #1727), covering at least said at least one electrode, (Figure 17 #1723), and said source wiring, (Figure 17 #1724); a gate wiring, (Figure 17 #1716), formed on said second insulating film, (Figure 17 #1727), electrically connected to said at least one electrode, (Figure 17 #1723); and a pixel electrode, (Figure 17 #1728), electrically connected to said semiconductor layer, (Figure 17 #1704-1712), wherein said gate wiring, (Figure 17 #1718),

and said pixel electrode, (Figure 17 #1728), are formed on said second insulating film, (Figure 17 #1727).

15. Referring to claim 24, a semiconductor device, wherein a material of said gate wiring comprises one or a plurality of elements selected from the group consisting of polySi, W, WSi, Al, Cu, Ta, Cr and Mo, (Col. 17 Lines 45-47 & Figures 9A & 11).

16. Referring to claim 25, a semiconductor device, wherein said first insulating film, (Figure 17 examiner's label #6), comprises a gate insulating film, (Figure 17 examiner's label #6).

17. Referring to claim 27, a semiconductor device, wherein said semiconductor device is one selected from the group consisting of a personal computer, a video camera, a portable information terminal, a digital camera, a digital video disk player, a portable telephone, an electronic book, a projector, a head mounted type display, and an electric game appliance, (Figures 33).

Allowable Subject Matter

18. Claims 2, 4, 7, 11, 13-14, 17, 22-23, & 26 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. Claims 28-37 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Victor A Mandala Jr. whose telephone number is (703) 308-6560. The examiner can normally be reached on Monday through Thursday from 8am till 6pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

VAMJ
August 7, 2003

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800